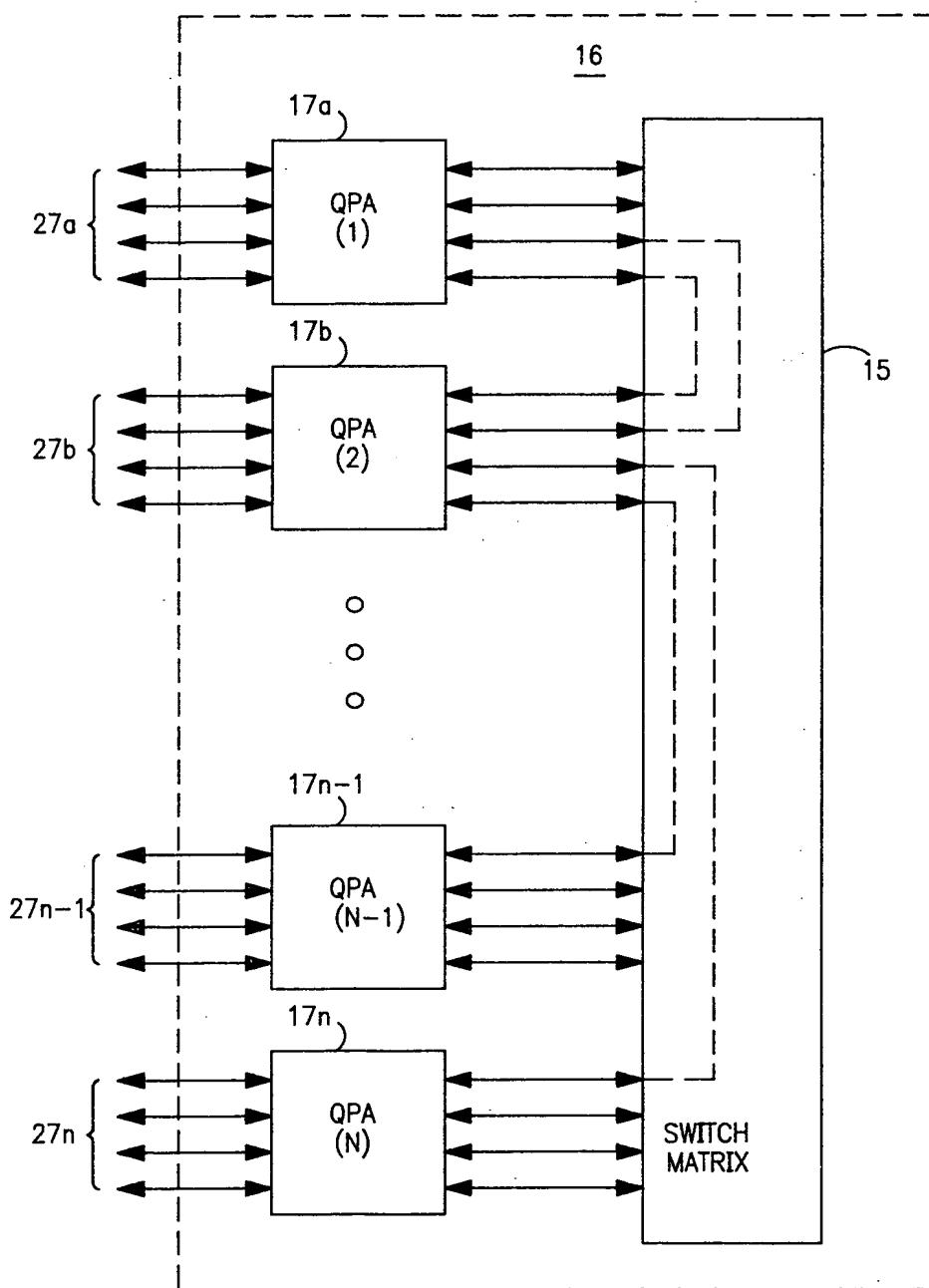


FIG. I  
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**FIG. 2**  
PRIOR ART

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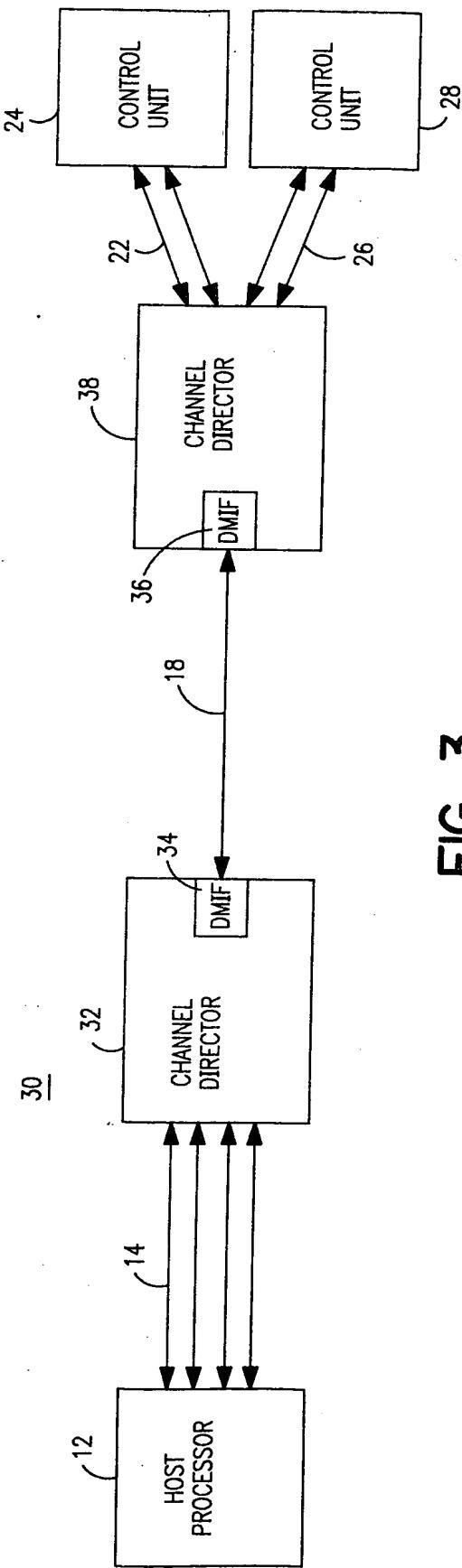


FIG. 3

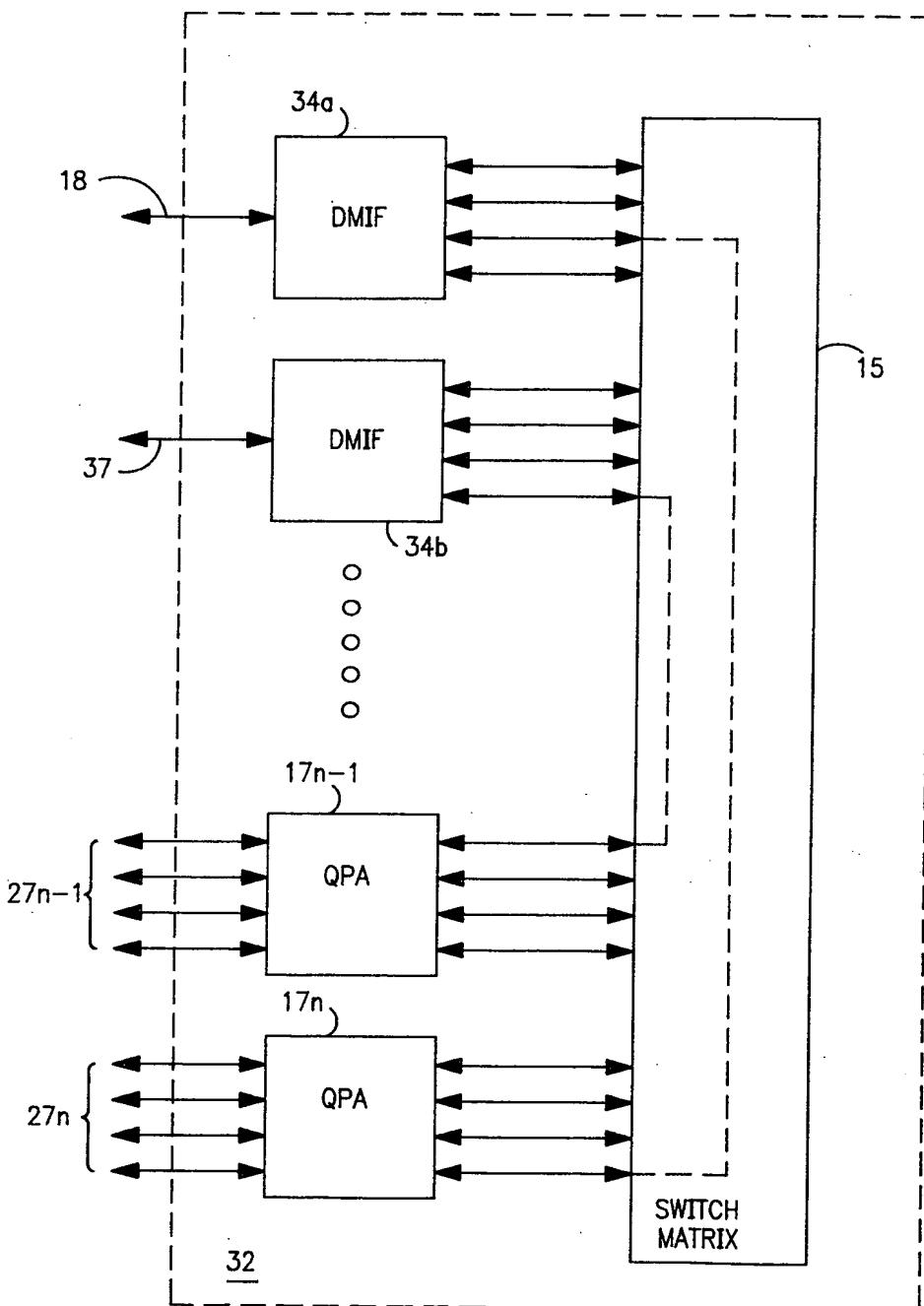


FIG. 4

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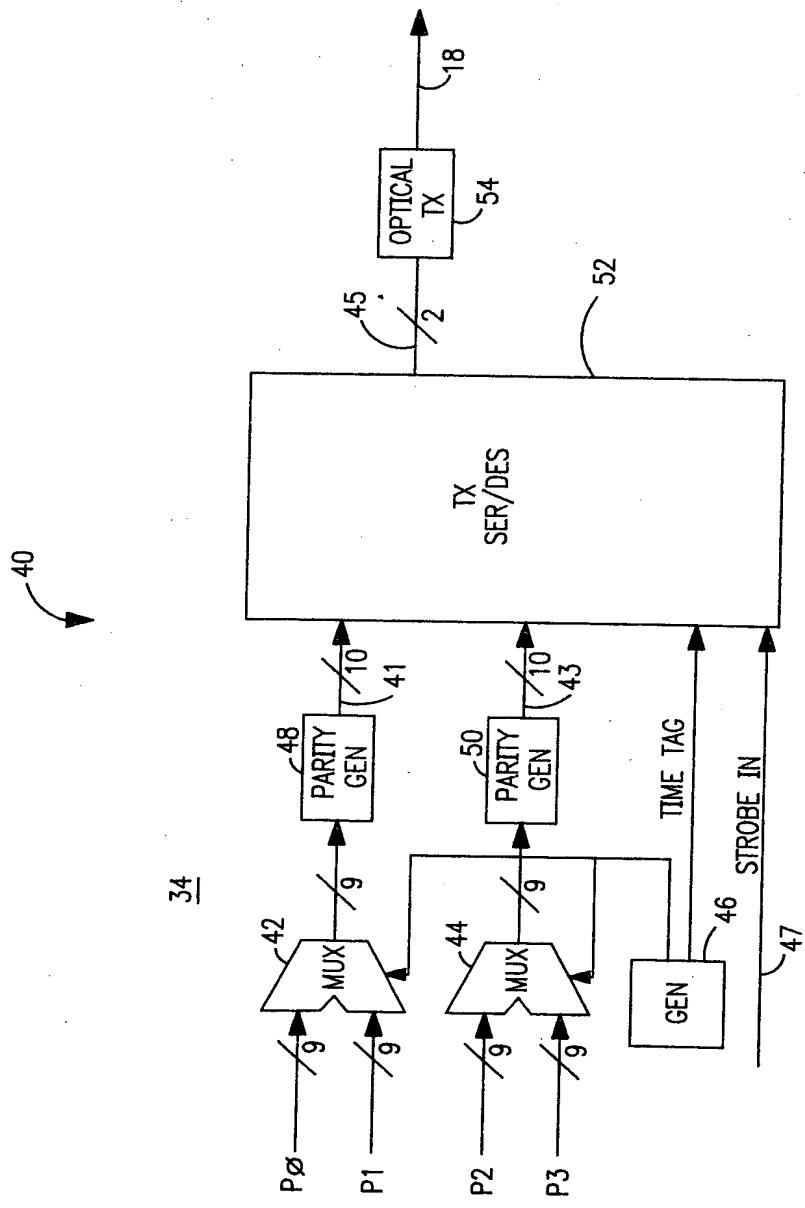


FIG. 5

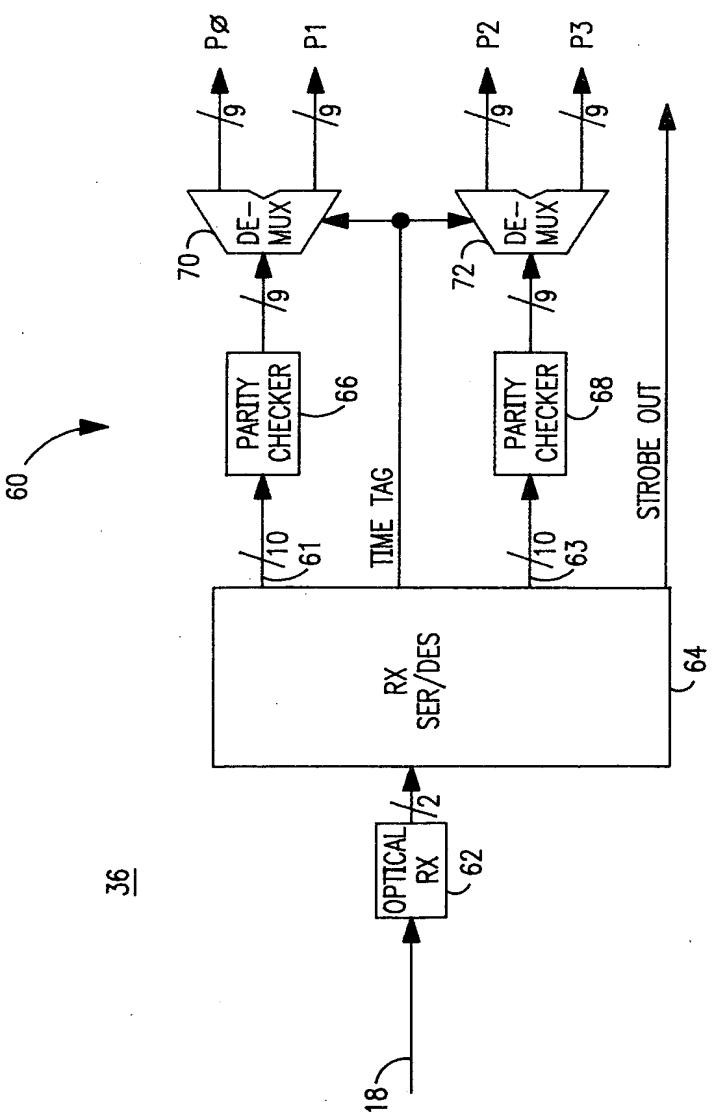


FIG. 6

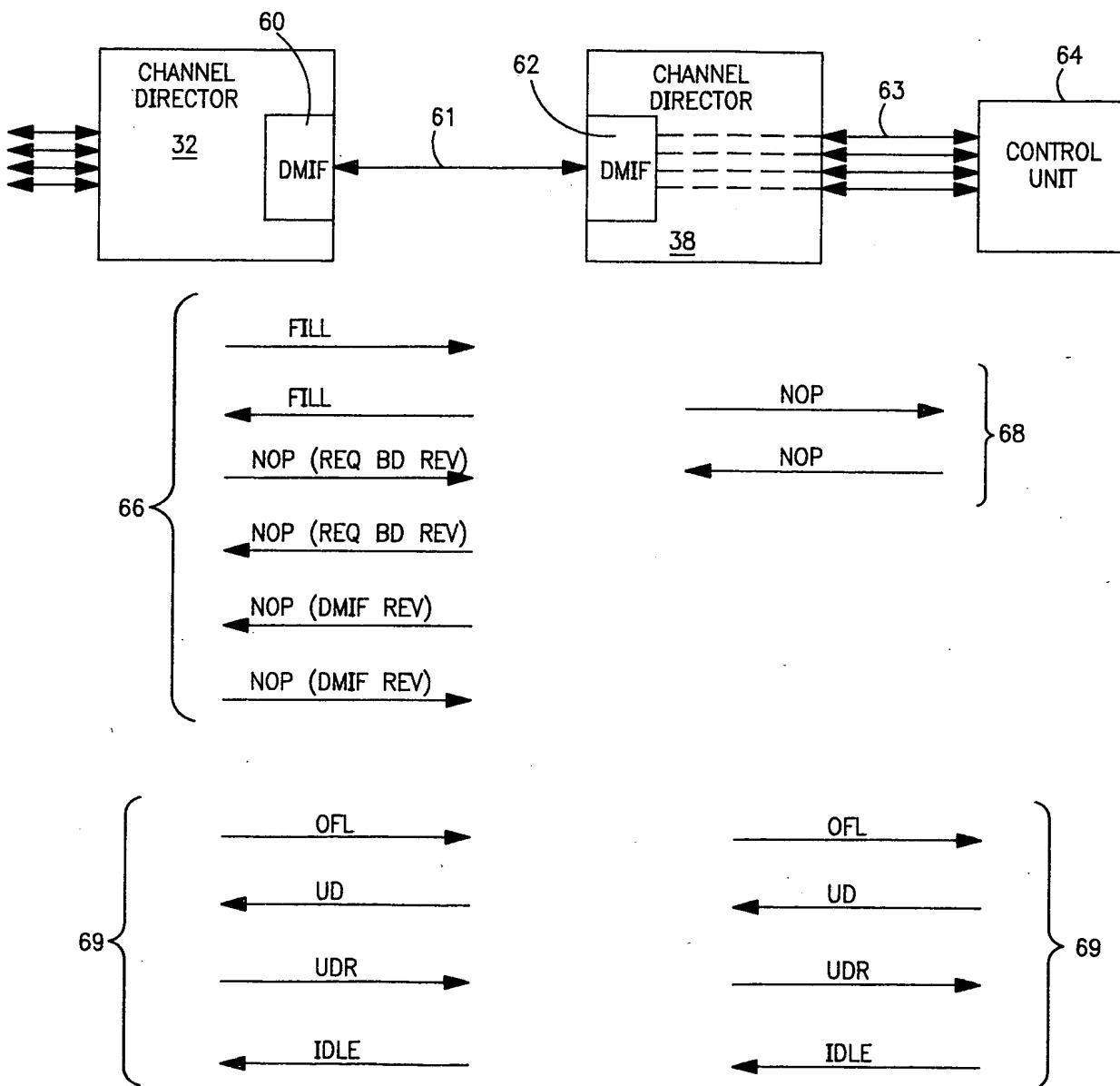


FIG. 7

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FIG. 8 shows a block diagram of a High Speed Linking Module. The diagram illustrates the internal architecture and data flow between various components.

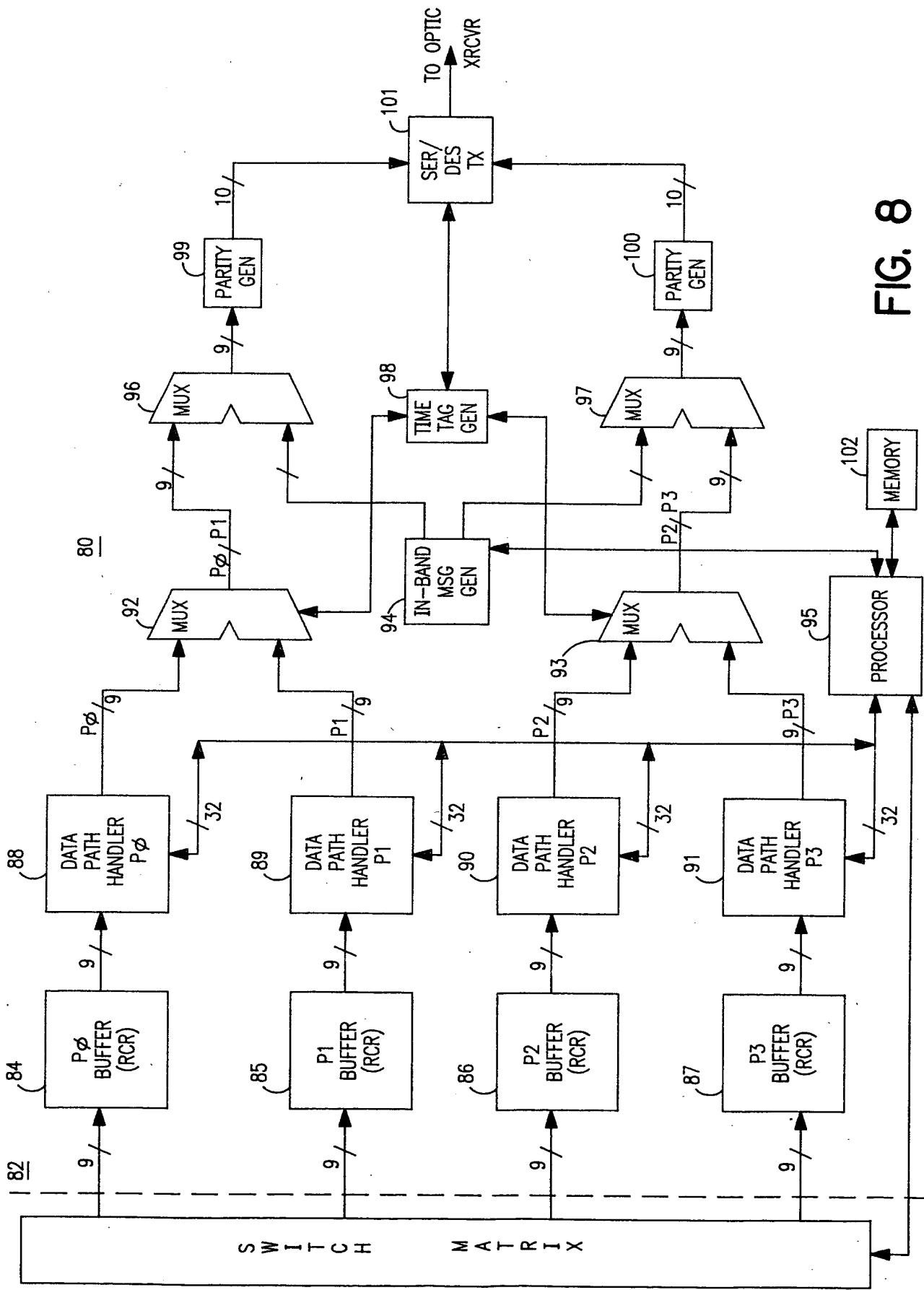


FIG. 8

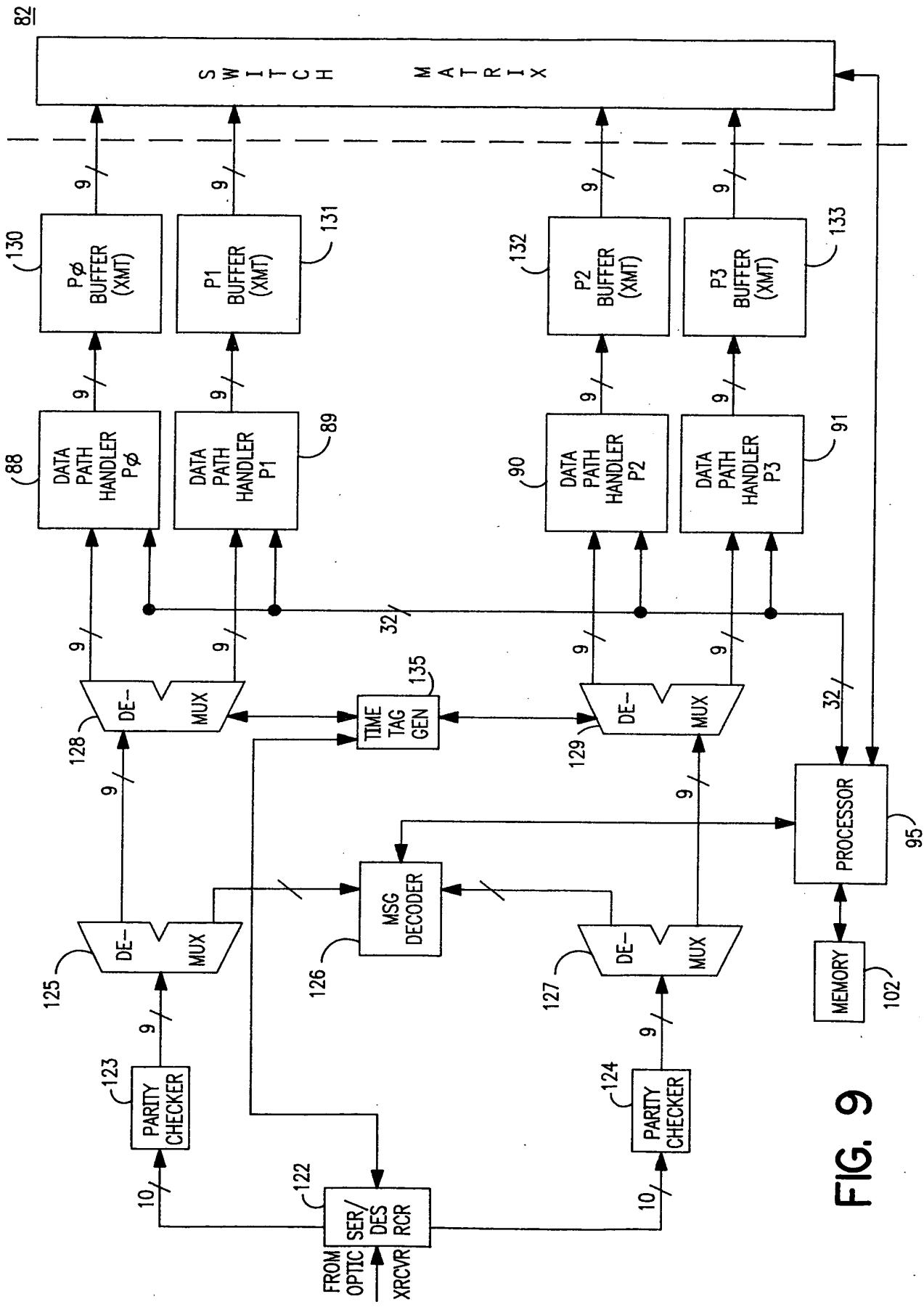


FIG. 9

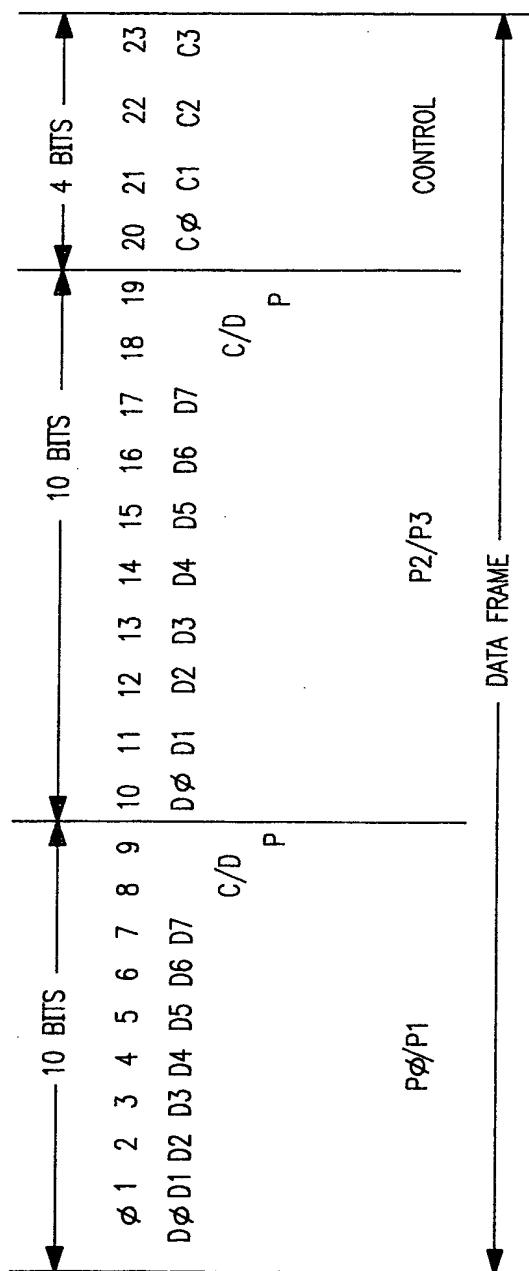


FIG. 10

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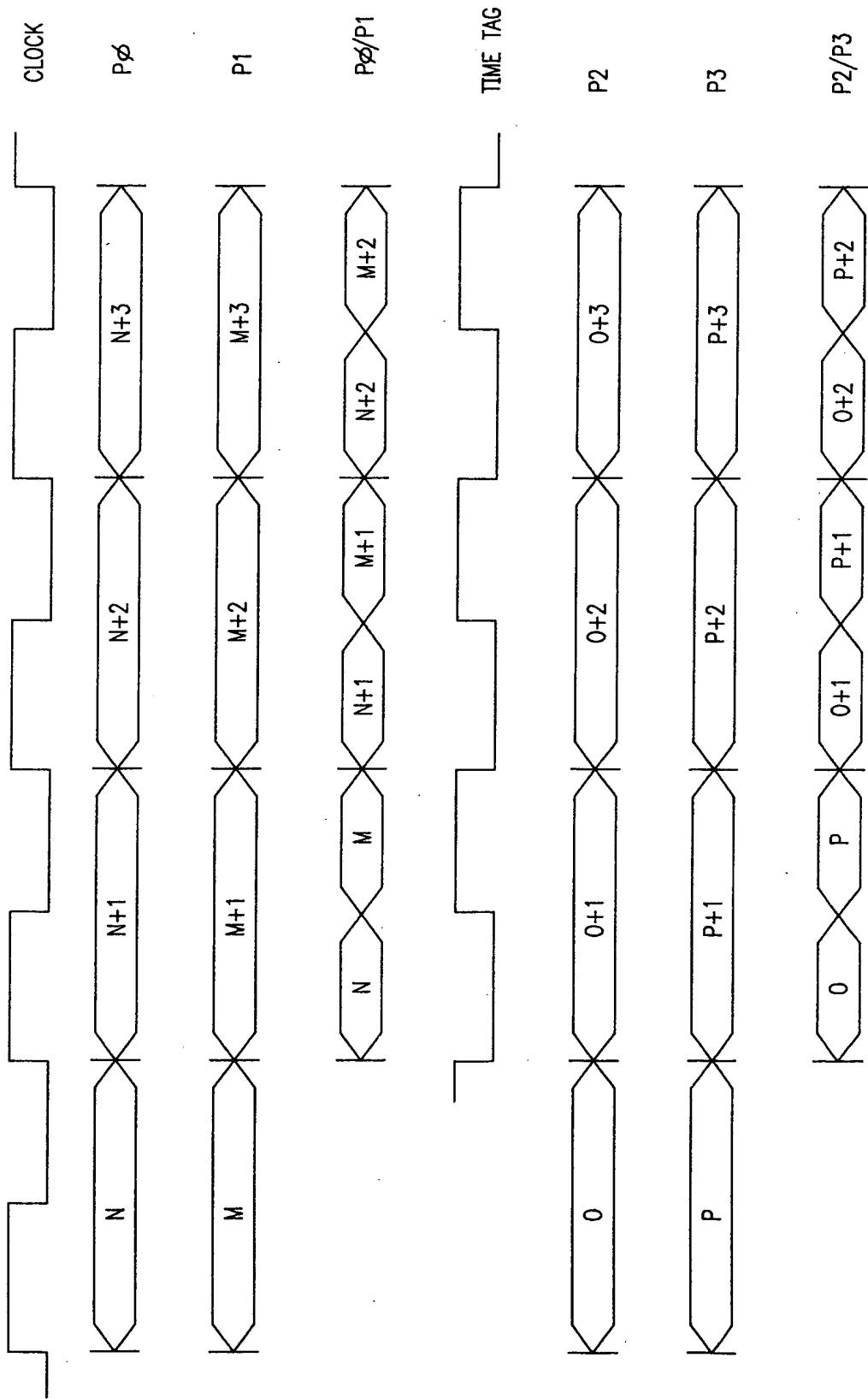


FIG. I I